REMARKS

Claims 8, 15, and 23-30 are all the claims presently pending in the application. Claims 8, 15 and 23 have been amended to more particularly define the invention. Claims 24-30 have been added to claim additional features of the invention. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment.

It is noted that the claim Amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability.

Claims 8, 15 and 23 stand rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Phillipossian (U.S. Pat. 5,316,965). Claims 8, 15 and 23 stand rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Weigand (U.S. Pat. 5,851,899). Claims 8, 15 and 23 stand rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Sahota (U.S. Pat. 5,923,993). Claims 8, 15 and 23 stand rejected under 35 U.S.C. § 102(a) as being clearly anticipated by DE 197 41 704 A1 (hereinafter "DE '704").

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor substrate with at least one trench having seam-less filler material having a surface which is substantially scratch-free and co-planar with a surface of the substrate.

Conventional substrates have shallow trench isolations which are formed with conformal chemical vapor deposition and planarized by chemical mechanical polishing (CMP) or Reactive Ion Etch (RIE). However, these processes necessarily form isolations which have, for example, seam defects and CMP scratches.

The claimed invention, on the other hand, has trenches with seam-less and scratch-free filler material which can not be formed using conventional methods.

II. THE PHILLIPOSSIAN, WEIGAND, CRONIN, SAHOTA AND DE '704 REFERENCES

The Examiner alleges that each of Phillipossian, Weigand, Cronin, Sahota and DE '704 teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by either Phillipossian, Weigand, Cronin, Sahota, or DE '704.

Phillipossian discloses a method for planarizing an isolation barrier which includes reducing the etch rate of the field oxide independently of the sacrificial oxide layer. The field oxide layer is implanted with nitrogen ions and then thermally annealed resulting in a hardened and densified field oxide. A sacrificial oxide layer is formed on the semiconductor top surface by thermal oxidation. Upon etching with HF, the etch rate of the hardened field oxide is significantly reduced relative to untreated field oxide. Thus, the exposed hardened field oxide is etched at about the same rate as the sacrificial oxide layer (Philipossian at Abstract).

Weigand discloses a method for filling shallow trench isolation (STI) trenches with an insulating material and planarizing the resulting structure to the level of adjacent portions of the integrated circuit. The method includes forming trenches in the non-active regions of the substrate, depositing a layer of oxide in the trenches and over the surface of the substrate, and removing the oxide from the active areas of the integrated circuit structure (Weigand at Abstract).

Cronin discloses a planarized semiconductor structure which is prepared by a method which involves the creation of a series of subminimum (i.e., 50 to 500 Angstroms thick) silicon pillars extending vertically upward from the base of a wide trench, and oxidizing the pillars. When the substrate is covered with a conformal CVD oxide, the pillars prevent the formation of a single deep depression above the trench (Cronin at Abstract).

Sahota discloses a method for fabricating dishing free shallow isolation trenches. The method includes the use of two nitride layers and an oxide layer formed by high density plasma oxidation, to provide isolation trenches free of dishing (Sahota at Abstract).

The DE '704 reference merely discloses a process for the production of isolations in a substrate. The process includes using a high density plasma to form isolations in a silicon

substrate (De '704 at Abstract).

However, none of these references teaches or suggests "at least one trench comprising seam-less filler material having a surface which is substantially scratch-free and co-planar with a surface of said substrate" as recited in claim 8. Neither does any of the references teach or suggest the novel method steps recited in claims 15 and 23.

As explained in the Application, conventional substrates have shallow trench isolations which are formed with conformal chemical vapor deposition and planarized by chemical mechanical polishing (CMP) or Reactive Ion Etch (RIE) (Application at page 1, line 15-page 2, line 8). However, the Application explains that "[d]ue to the nature of conformal LPCVD TEOS deposition, seams are generally present in the LPCVD TEOS [low pressure chemical vapor deposition tetraethylorthosilane] filled shallow trench isolation region. The seams become a major problem as the device dimensions scale downward and the aspect ratio of the STI increases" (Application at page 2, lines 15-18). Further, REI and CMP result in defects such as particulate contamination, CMP scratches and chatter marks (Application at page 12, lines 20-21). In other words, these processes necessarily form isolations which have seam defects, scratches and chatter marks.

The claimed substrate, on the other hand, has a seam-less filler material which can not be formed using conventional methods (Application at Figure 7; page 10, lines 8-10). The Application explains that a seam-less filler material may be formed, for example, of a non-conformal high density plasma oxide (Application at page 5, line 4-page 11, line 3). Further, the non-conformal high density plasma oxide may be formed substantially co-planar with a surface of the substrate surface, for example, without the use of RIE or CMP (Application at page 12, lines 16-20). Therefore, unlike conventional semiconductor substrates, the claimed substrate may have shallow trench isolations filled with seam-less filler material with a substantially scratch-free surface (Application at page 12, line 20-page 13, line 1).

Clearly, none of the references teaches or suggests these novel features. Indeed, Phillipossian does not even recognize the problem of seam defects in the filler material which is a problem that the claimed device seeks to address. Further, like the methods discussed in the background section of the Application, the Phillipossian method fills trenches using LPCVD TEOS (Phillipossian at col. 3, lines 55-59; col. 4, lines 42-55). In other words,

nowhere does Phillipossian teach or suggest, for example, shallow trench isolations formed by non-conformal high density plasma which may be used to form the claimed invention. Therefore, Phillipossian cannot necessarily teach or suggest a trench having "seam-less filler material" as in the claimed substrate.

Further, Weigand specifically discloses a CMP step in the formation of the shallow trench isolation (Weigand at col. 6, lines 19-46). Therefore, the Weigand method necessarily results in CMP scratches in a surface of the shallow trench isolations.

Like Phillipossian, Cronin teaches the use of a conformal CVD oxide in forming the trench fill (Cronin at col. 1, lines 49-62). Further, Cronin also teaches a CMP planarization step (Cronin at col. 3, line 12-43). Therefore, the Cronin method necessarily results in a substrate having a filler material with seams and scratches, unlike the claimed substrate.

In addition, like Weigand, Sahota specifically discloses a CMP step in the formation of the shallow trench isolation (Sahota at col. 3, lines 40-58). Therefore, the Weigand method necessarily results in CMP scratches in a surface of the shallow trench isolations.

Further, as noted above, DE '704 merely teaches forming isolations in a silicon substrate using high density plasma. However, like Weigand and Sahota, DE '704 specifically teaches chemical mechanical polishing which necessarily results in CMP scratches on a surface of the isolations.

Therefore, Applicant submits that neither Phillipossian, Weigand, Cronin, Sahota nor DE '704 teaches or suggests each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw these rejections.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 8, 15 and 23-30, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 11/30/01

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 24-30 have been added.

The claims were amended as follows:

8. (Amended) A semiconductor substrate comprising:

at least one trench comprising seam-less filler material having a surface which is substantially scratch-free and co-planar with a surface of said substrate [having a planarized trench region formed according to the method of claim 1].

15. (Amended) A semiconductor substrate having a planarized trench region formed according to a [the] method comprising:

forming a pad on a surface of said substrate;

forming at least one trench in said substrate;

applying a filler material by high density plasma method in said at least one trench and on said pad;

selectively removing said filler material on said pad so as to separate said filler material in said at least on trench and said filler material on said surface by an exposed area of said pad, and

removing said filler material on said pad [of claim 9].

23. (Amended) A semiconductor substrate having a planarized structure formed according to a [the] method comprising:

forming a pad on a surface of said substrate;

forming at least one trench in said substrate;

applying a filler material by high density plasma method in said at least one trench and on said pad, said filler material filling said at least one trench to a predetermined height;

selectively removing said filler material on said pad so as to separate said filler material in said at least on trench and said filler material on said surface by an exposed area of said pad, and

removing said filler material on said pad while allowing said filler material in said at

least one trench to remain filled to said predetermined height [of claim 16].